19-2318; Rev 0; 1/02

MAXIM

Precision Resistor Network for Programmable Instrumentation Amplifiers

General Description

The MAX5426 is a precision resistor network optimized for use with programmable instrumentation amplifiers. The MAX5426 operates from dual ±5V to ±15V supplies and consumes less than 40µA of supply current. Designed to be used in the traditional three op amp instrumentation amplifier topology, this device provides noninverting gains of 1, 2, 4, and 8 that are accurate to 0.025% (A-grade), 0.09% (B-grade), or 0.5% (C-grade) over the extended temperature range (-40°C to +85°C). The MAX5426 is available in the 6.4mm × 5mm 14-pin TSSOP package.

Applications

General-Purpose Programmable Instrumentation Amplifiers

Gain Control in RF Power Amplifiers

Precision Dual Attenuator

Features

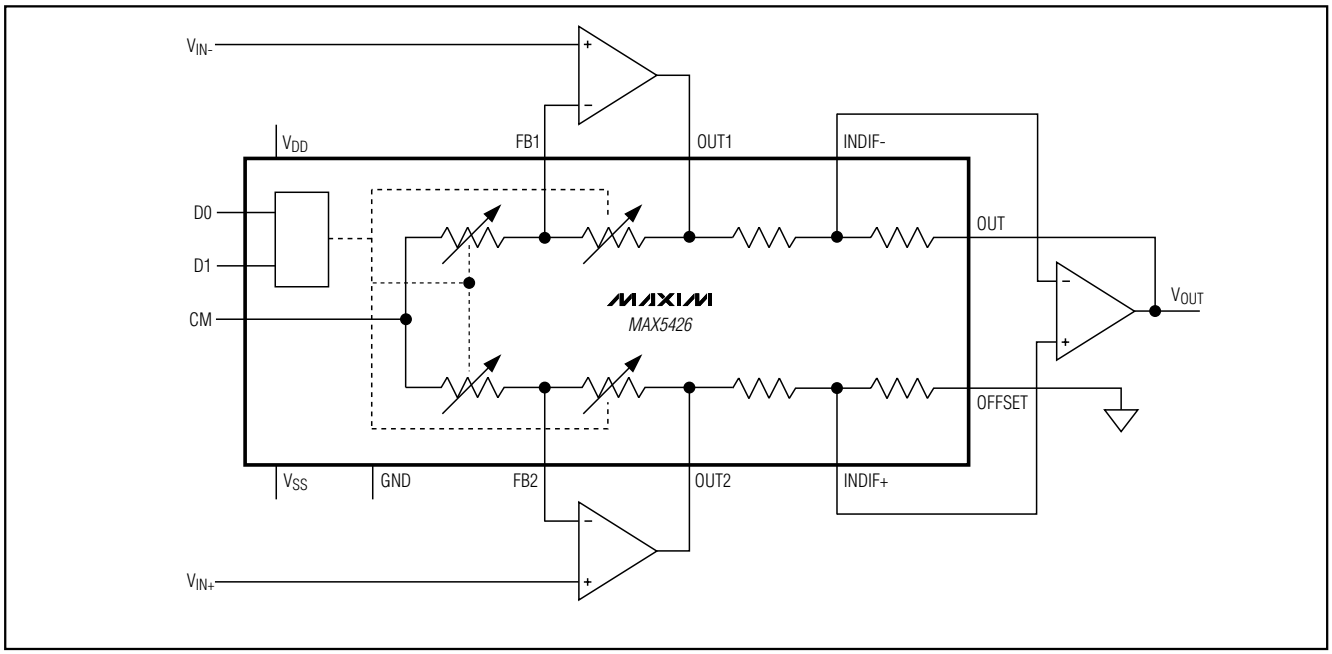
- **Differential Gains: AV = 1, 2, 4, 8**
- **Gain Accurate to 0.025%, 0.09%, or 0.5%**
- **Dual Supply ±5V to ±15V Operation**
- **Low 36µA Supply Current**
- **Simple CMOS/TTL Logic Compatible 2-Wire Parallel Interface**
- **Space-Saving 14-Pin TSSOP Package (6.4mm × 5mm)**
- **OFFSET Pin Available to Offset the Output of the Differential Amplifier**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	GAIN
MAX5426AEUD	-40°C to +85°C	14 TSSOP	0.025%
MAX5426BEUD	-40°C to +85°C	14 TSSOP	0.09%
MAX5426CEUD	-40°C to +85°C	14 TSSOP	0.5%

Pin Configuration and Functional Diagram appear at end of data sheet.

Typical Operating Circuit



Precision Resistor Network for Programmable Instrumentation Amplifiers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +17V
V_{SS} to GND.....-17V to +0.3V
D0, D1 to GND .....-0.3V to (V_{DD} + 0.2V)
D0, D1 to GND (V_{DD} > +6V) .....-0.3V to +6.0V
All Other Pins to GND .....(V_{SS} - 0.3V) to (V_{DD} + 0.2V)
Maximum Current Into V_{DD}, V_{SS}, D1, D0 .....±50mA
Maximum Current from OUT1 to CM or OUT2 .....±0.72mA
Maximum Current from OUT1 to INDIF- or OUT.....±0.72mA
Maximum Current from OUT2 to INDIF+ or OFFSET.....±0.72mA
Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{SS} = -15V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Range Accuracy (Notes 1, 2)		MAX5426A		0.004	0.025	%
		MAX5426B		0.025	0.090	
		MAX5426C		0.080	0.500	
Capacitance at Analog Pins	C_{ANALOG}			5		pF
Differential CMRR (Notes 1, 2)		Gain = 1		79		dB
		Gain = 2		85		
		Gain = 4		91		
		Gain = 8		97		
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{LKG}	D1 = D0 = 0 or logic high			10	µA
EQUIVALENT RESISTANCES						
Resistance Between OUT1 and OUT2	R_{OUT1}, R_{OUT2}			56		kΩ
Resistance Between OUT1 and INDIF-	R_{OUT1}, R_{INDIF-}			26		kΩ
Resistance Between INDIF- and OUT	R_{INDIF-}, R_{OUT}			26		kΩ
Resistance Between OUT2 and INDIF+	R_{OUT2}, R_{INDIF+}			26		kΩ
Resistance Between INDIF+ and OFFSET	R_{INDIF+}, R_{OFFSET}			26		kΩ
Resistance Between OUT1 and FB1	R_{OUT1}, R_{FB1}	Gain = 1		0		kΩ
		Gain = 2		15		
		Gain = 4		22		
		Gain = 8		26		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +15V, V_{SS} = -15V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resistance Between FB1 and FB2 (Note 3)	R_{FB1}, R_{FB2}	Gain = 2		29		kΩ
		Gain = 4		15		
		Gain = 8		7		
Resistance Between OUT2 and FB2	R_{OUT2}, R_{FB2}	Gain = 1		0		kΩ
		Gain = 2		15		
		Gain = 4		22		
		Gain = 8		26		
Input Impedance at FB1	Z_{FB1}			0		kΩ
Input Impedance at FB2	Z_{FB2}			0		kΩ
Input Impedance at OUT1 (Note 4)	Z_{OUT1}	Gain = 1		0		kΩ
		Gain = 2		9.5		
		Gain = 4		12		
		Gain = 8		13		
Input Impedance at OUT2 (Note 4)	Z_{OUT2}	Gain = 1		0		kΩ
		Gain = 2		9.5		
		Gain = 4		12		
		Gain = 8		13		
Input Impedance at INDIF+ (Note 4)	Z_{INDIF+}			0		kΩ
Input Impedance at INDIF- (Note 4)	Z_{INDIF-}			0		kΩ
Input Impedance at OUT (Note 4)	Z_{OUT}			26		kΩ
Input Impedance at OFFSET (Note 4)	Z_{OFFSET}			26		kΩ
POWER REQUIREMENTS						
Positive Power-Supply Voltage	V_{DD}		4.75		15.75	V
Negative Power-Supply Voltage	V_{SS}		-15.75		-4.75	V
Positive Supply Current	I_{DD}	D1 = D0 = 0		10		μA
		D1 = D0 = 5V		36	80	
Negative Supply Current	I_{SS}			0.01	10	μA
TIMING REQUIREMENTS						
Switching Time (Note 5)	$t_{SWITCHING}$	(Figure 3)		60		ns

Note 1: Total error when configured as instrumentation amplifier. Assumes ideal op amps.

Note 2: Each stage (input stage and output stage) is tested for accuracy separately and combined to give the total gain accuracy. The input stage is tested as follows: OUT1 = 10V, OUT2 = 0. Output stage is tested as follows OUT1 = 10V, OUT2 = 0 and OUT2 = 10V, OFFSET = 0.

Note 3: Gain of 1 configuration is open circuit (infinite impedance).

Note 4: Equivalent load at each pin is calculated according to instrumentation amplifier configuration and assumes ideal op amps.

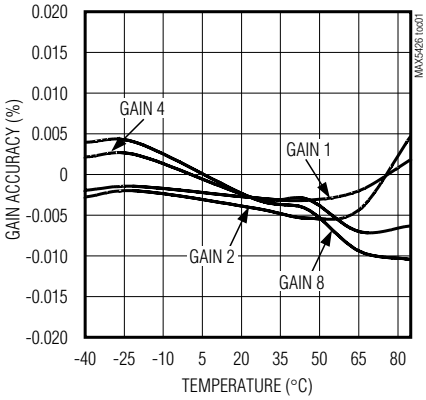
Note 5: See *Timing Diagram.*

Precision Resistor Network for Programmable Instrumentation Amplifiers

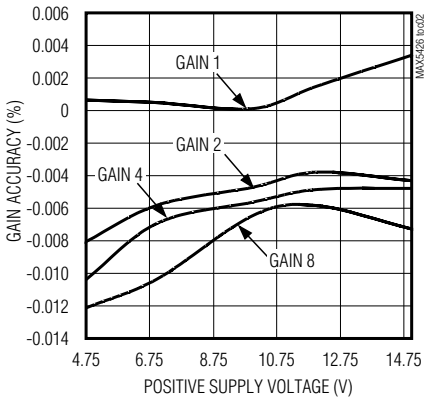
Typical Operating Characteristics

(V_{DD} = +15V, V_{SS} = -15V, T_A = +25°C, unless otherwise noted.)

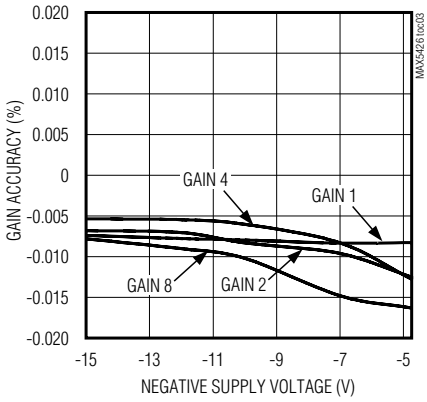
MAX5426A GAIN ACCURACY vs. TEMPERATURE



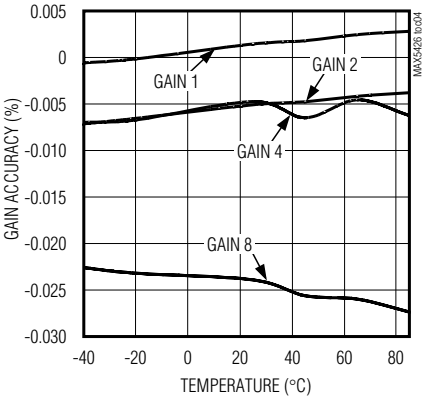
MAX5426A GAIN ACCURACY vs. POSITIVE SUPPLY VOLTAGE



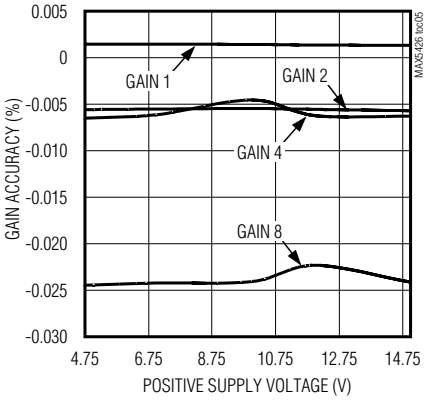
MAX5426A GAIN ACCURACY vs. NEGATIVE SUPPLY VOLTAGE



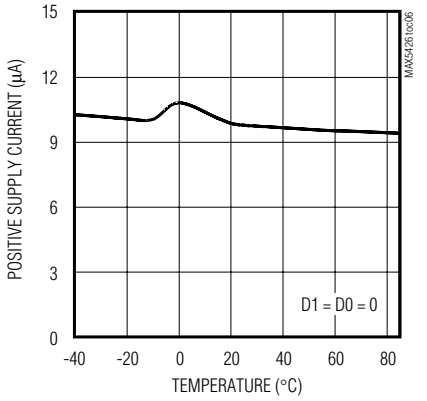
MAX5426B GAIN ACCURACY vs. TEMPERATURE



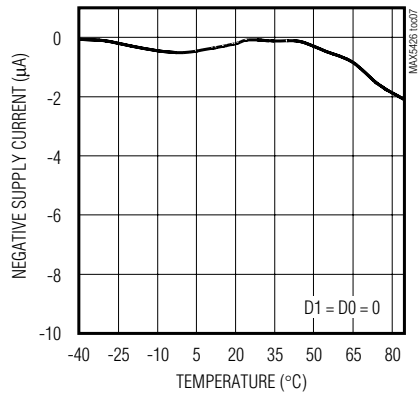
MAX5426B GAIN ACCURACY vs. POSITIVE SUPPLY VOLTAGE



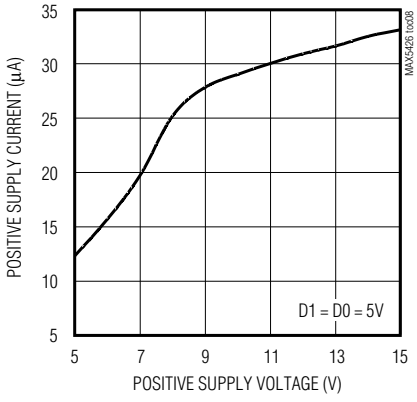
POSITIVE SUPPLY CURRENT vs. TEMPERATURE



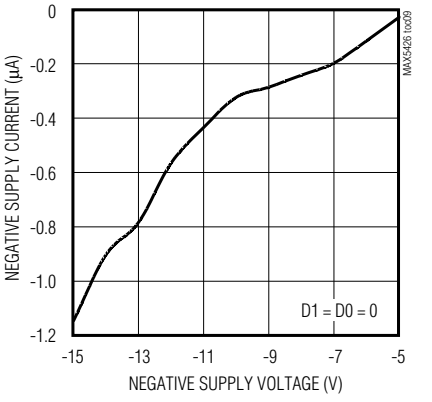
NEGATIVE SUPPLY CURRENT vs. TEMPERATURE



POSITIVE SUPPLY CURRENT vs. POSITIVE SUPPLY VOLTAGE



NEGATIVE SUPPLY CURRENT vs. NEGATIVE SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Power Supply. Bypass V_{DD} to GND with a 0.1µF capacitor.
2	GND	Ground
3	V_{SS}	Negative Power Supply. Bypass V_{SS} to GND with a 0.1µF capacitor.
4	FB2	First Stage Positive Input Terminal Resistor. Connect to the inverting terminal of the second input buffer (see Figure 1).
5	OUT2	First Stage Positive Output Terminal Resistor. Connect to the output terminal of the second input buffer.
6	OFFSET	Second Stage Offset Terminal. Connect to a DC voltage to offset the output of the differential amplifier.
7	INDIF-	Second Stage Negative Input Terminal Resistor. Connect to the inverting input terminal of the differential op amp.
8	INDIF+	Second Stage Positive Input Terminal Resistor. Connect to the noninverting input terminal of the differential op amp.
9	OUT	Second Stage Output Terminal, Final Output Terminal
10	OUT1	First Stage Negative Output Terminal of Resistor. Connect to the output terminal of the first input buffer.
11	FB1	First Stage Negative Input Terminal of Resistor. Connect to the inverting input terminal of the first input buffer.
12	CM	Common-Mode Voltage. CM is the input common-mode voltage of the instrumentation amplifier. Typically varies ±1% of input common-mode voltage.
13, 14	D0, D1	Digital Inputs. See Table 1.

Detailed Description

The MAX5426 is a precision resistor network with low temperature drift and high accuracy that performs the same function as a precision resistor array and CMOS switches. Operationally, this device consists of fixed resistors and digitally controlled variable resistors that provide differential gains of 1, 2, 4, and 8 (see *Functional Diagram*). The MAX5426 provides gains accurate to 0.025% (MAX5426A), 0.09% (MAX5426B) or 0.5% (MAX5426C).

The MAX5426 is ideal for programmable instrumentation amplifiers. An offset pin is available to apply a DC offset voltage to the output of the differential amplifier. Pin CM is the common-mode input voltage and can be buffered and connected to the common-mode input of the instrumentation amplifier (usually the shield of the input cable to reduce the effects of cable capacitance and leakage).

Digital Interface Operation

The MAX5426 features a simple two-bit parallel programming interface. D1 and D0 program the gain setting according to the *Logic-Control Truth Table* (see Table 1). The digital interface is CMOS/TTL logic compatible.

Timing Diagram

Figure 3 shows the timing diagram of MAX5426 for two cases. In case 1, the differential input changes are at OUT1 and OUT2, while the voltage settling is observed at FB1 and FB2. The settling time (t_{SETTLE}) is defined as the time for the output voltage (from the change in the input) to reach (and stay) within 0.02% of its final value.

In case 2, the differential inputs (OUT1 and OUT2) are at constant voltages, while D1 and D0 are varied (for example from 01 to 10) to make a change in the gain. No op amps are used in these cases.

Table 1. Logic-Control Truth Table

DIGITAL INPUTS		
D1	D0	GAIN
0	0	1
0	1	2
1	0	4
1	1	8

Precision Resistor Network for Programmable Instrumentation Amplifiers

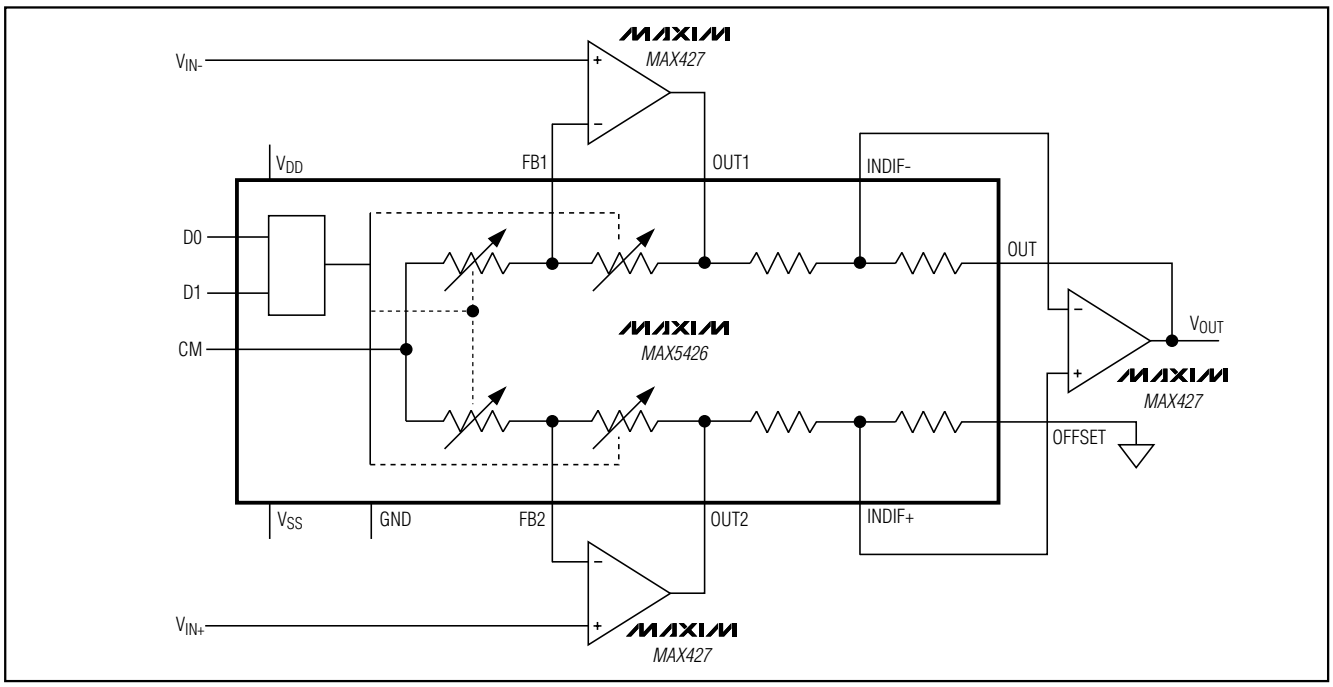


Figure 1. Programmable Instrumentation Amplifier Using MAX5426

Applications Information

The MAX5426 is ideal for programmable instrumentation amplifier applications. The typical application circuit of Figure 1 uses the MAX5426 in classical instrumentation amplifier configurations. Two digital inputs set the gain to 1, 2, 4, or 8.

Op Amp Selection Guidelines

Selection of an op amp for instrumentation amplifier circuits depends on the accuracy requirements of the specific application. General guidelines are to choose an op amp with sufficient open-loop gain, low input-offset voltage, and a high common-mode rejection ratio.

High open-loop gain is needed to increase the gain accuracy, while low input-offset voltage and low input-offset current help meet gain and offset requirements.

Other parameters such as low input capacitance, low input bias current, high input common-mode range, and low noise often need to be considered for a wide input voltage range stability and AC considerations. The MAX427 is an excellent choice to use with the MAX5426.

Stereo Audio-Taper Attenuator

Figure 2 shows the application of the MAX5426 as a dual attenuator that can be used in stereo audio systems.

Power Supplies and Bypassing

The MAX5426 operates from dual ±5V to ±15V supplies. In many applications the MAX5426 does not require bypassing. If power-supply noise is excessive, bypass V_{DD} and V_{SS} with 0.1µF ceramic capacitors to GND.

Layout Concerns

For best performance, reduce parasitic board capacitance by minimizing the circuit board trace from amplifier outputs to inverting inputs. Also choose op amps with low input capacitance.

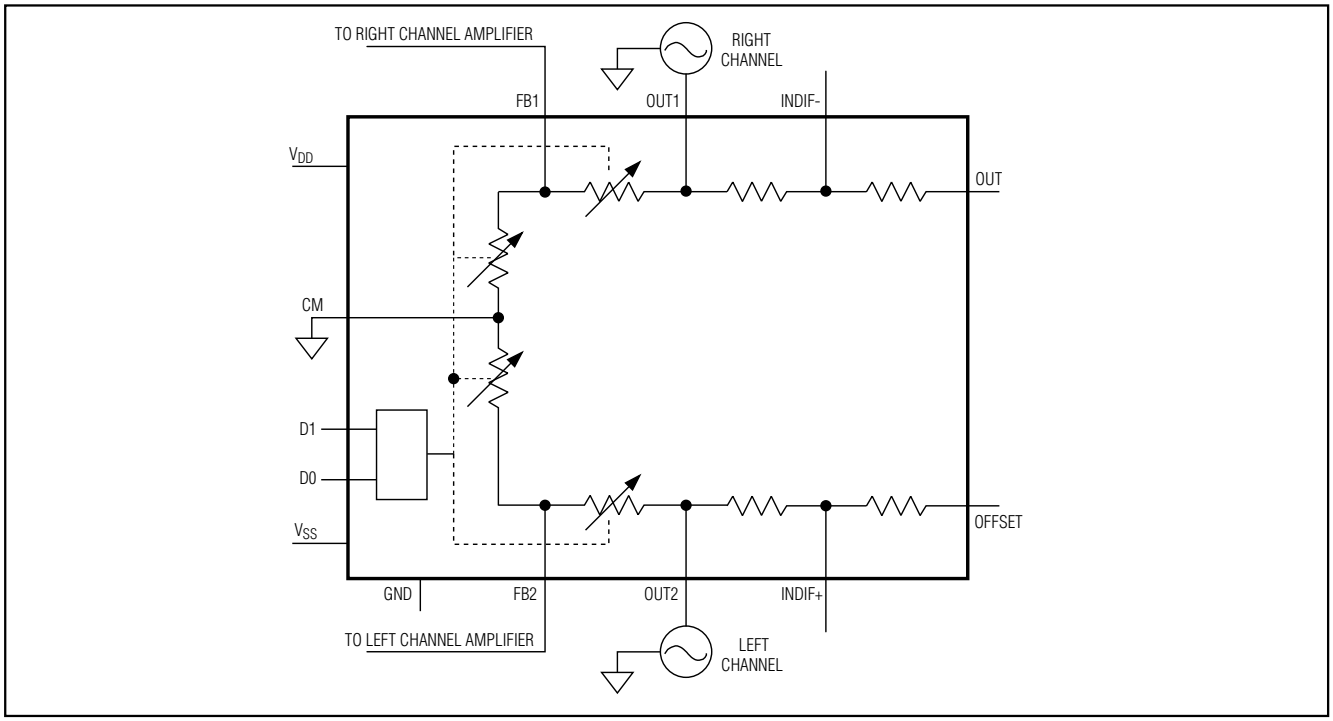


Figure 2. Stereo Audio-Taper Attenuator

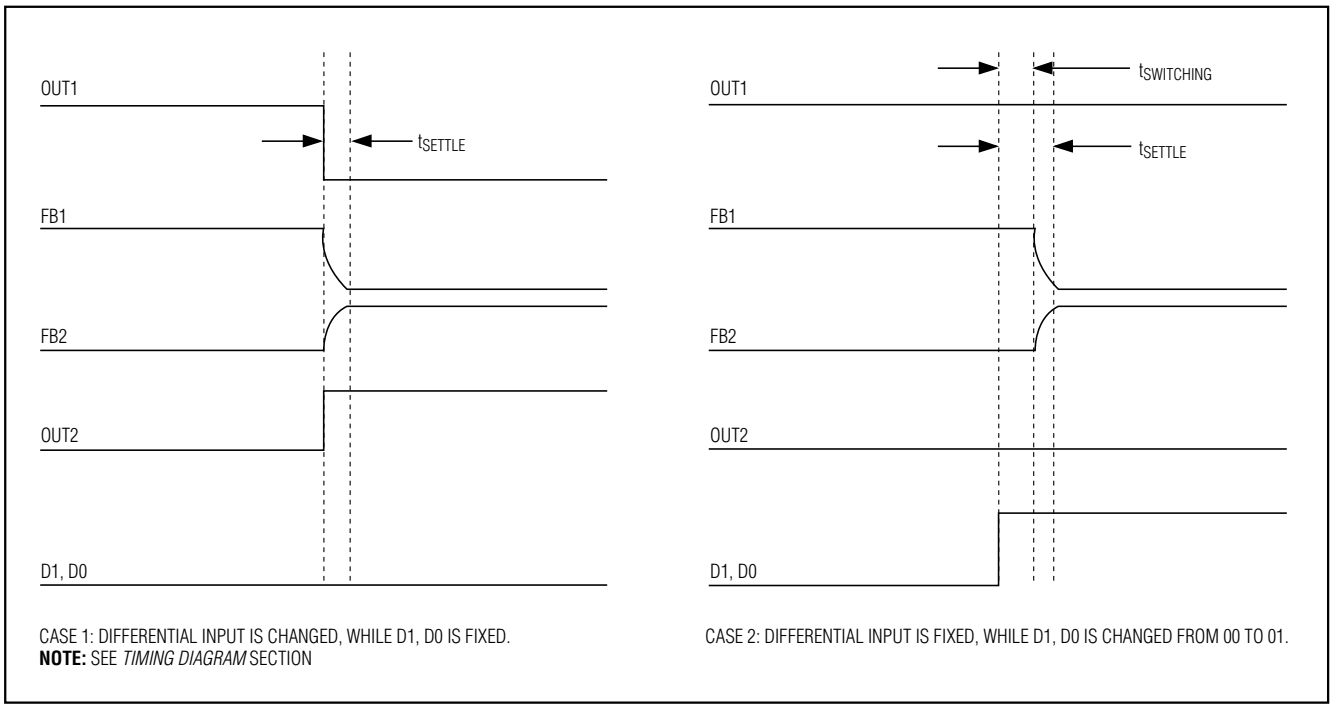
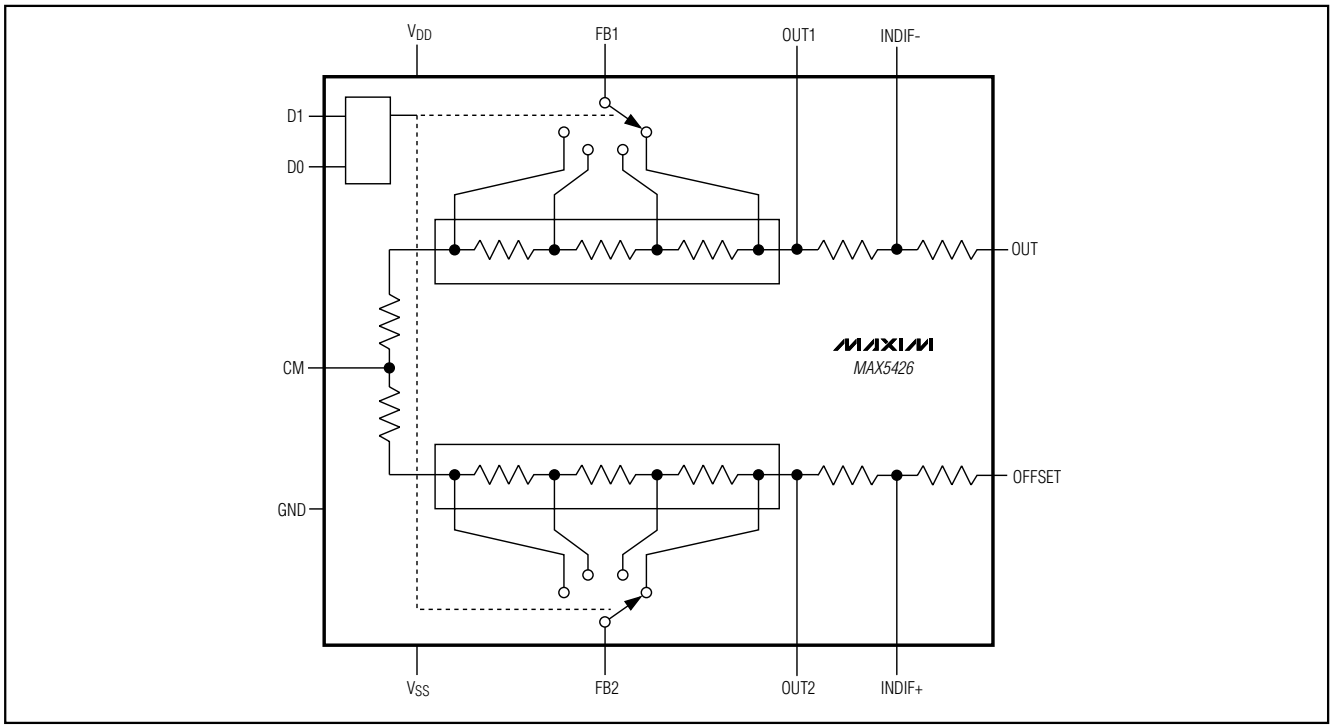


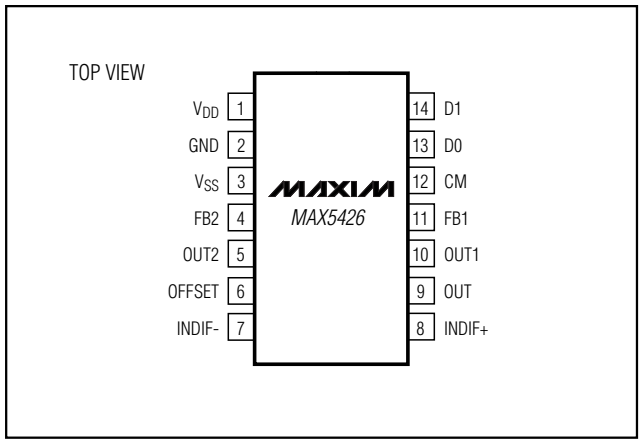
Figure 3. Timing Diagram

Precision Resistor Network for Programmable Instrumentation Amplifiers

Functional Diagram



Pin Configuration



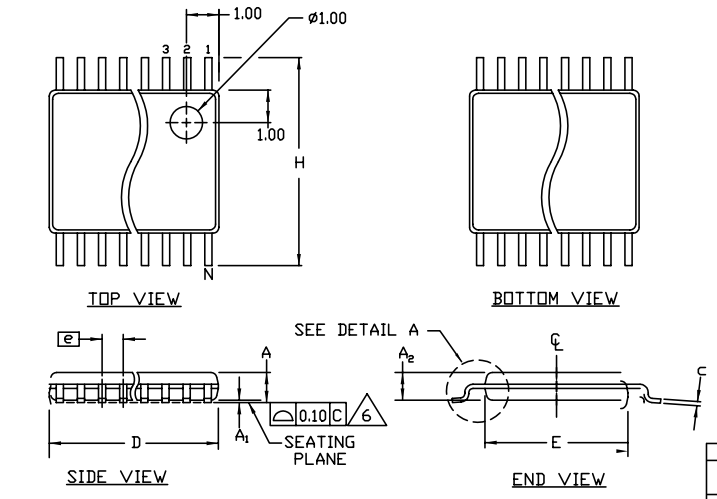
Chip Information

TRANSISTOR COUNT: 126

PROCESS TECHNOLOGY: BICMOS

Package Information

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	E	1/1